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| 10/530,899 | 10/26/2005 | Eric Diehl | PF020137 | 9210 |

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| EXAMINER | |
|---|---|
| VERDERAMO III, RALPH | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/530,899 | DIEHL, ERIC | |
| | Examiner | Art Unit | |
| | Ralph A. Verderamo III | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1 – 3 and 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi et al. "Tradeoffs in Two-Level On-Chip Caching" (herein after referred to as Jouppi) in view of Bryant et al. US Patent No. 4008460 (herein after referred to as Bryant).

Regarding claim 1, Jouppi describes a device for memorizing a list of items, said device being adapted to memorize an item presented thereto, said device being capable of memorizing N items (Two level exclusive caching, page 43, section 8) (Sizes of the cache levels are described, page 35, section 2.1), N being a natural integer, comprising: a first memory adapted to memorize a maximum of M items that were presented to said device (Desired lines are

loaded directly to first level cache (page 43, section 8)), M being a natural integer less than N (size of first level cache being less than the total size of both first and second level cache (page 35, section 2.1)); a second memory adapted to memorize N-M second items, each of N-M items being different from each of said M items (Under this scheme a mapping conflict in both first-level and second-level direct-mapped caches will give rise to "exclusion"; that is, the data involved in the mapping conflict will exist in one level of the hierarchy or the other, but not both (page 43, section 8)), a victim of said M items in said first memory being moved to said second memory (the first-level victim is sent to the second level cache (page 43, section 8)); means for randomly selecting one of said second items memorized in the second memory and for removing the selected item if said second memory already contains N-M items when said first item is presented for memorization in said device (Pseudo-random replacement (page 35, section 2.1)) (page 43, section 8); and means to memorize a first item in said device (page 43, section 8). Jouppi does not specifically describe that the first memory stores the M items that were last presented to said device, that an oldest of said M items in said first memory being moved to said second memory if said first memory already contains M items when a first item is presented for memorization or that the first item becomes a newest of said M items in said first memory.

Bryant describes that one replacement algorithm is LRU (least recently used), whereby the block in the buffer which was referenced least recently (i.e.

longest not used) is assumed to be the least important, and therefore can be written over, i.e. replaced with minimum system performance impact (column 1, lines 13 – 18). It is further known that in an LRU replacement scheme that an item that has just been referenced becomes the most recently used. Items removed from would be the oldest items that have been least recently used.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a LRU replacement algorithm as described by Bryant with the first memory of Jouppi because LRU provides performance benefits by replacing items which have been deemed to be least important because they have been least recently used (column 1, lines 13 – 18).

Regarding claim 2, Jouppi in view of Bryant describe the device according to claim 1 (see above), said device being adapted to supply information indicating whether said first item is already present in said device (cache hit (Jouppi, page 43, section 8 and page 37, section 2.5)).

Regarding claim 3, Jouppi in view of Bryant describe the device according to claim 1 (see above), said device being adapted to contain only one copy of each item memorized (two-level exclusive caching (Jouppi, page 43, section 8)).

Regarding claim 6, Jouppi describes a method of memorizing an item in a device adapted to memorize an item presented thereto, said device being capable of memorizing N items (Two level exclusive caching, page 43, section 8) (Sizes of the cache levels are described, page 35, section 2.1), N being a natural integer, comprising: a first memory adapted to memorize a maximum of M items

that were presented to said device (Desired lines are loaded directly to first level cache (page 43, section 8)), M being a natural integer less than N (size of first level cache being less than the total size of both first and second level cache (page 35, section 2.1)); a second memory adapted to memorize N-M second items, each of N-M items being different from each of said M items (Under this scheme a mapping conflict in both first-level and second-level direct-mapped caches will give rise to "exclusion"; that is, the data involved in the mapping conflict will exist in one level of the hierarchy or the other, but not both (page 43, section 8)), a victim of said M items in said first memory being moved to said second memory (the first-level victim is sent to the second level cache (page 43, section 8)); means for randomly selecting one of said second items memorized in the second memory and for removing the selected item if said second memory already contains N-M items when said first item is presented for memorization in said device (Pseudo-random replacement (page 35, section 2.1)) (page 43, section 8); and means to memorize a first item in said device (page 43, section 8) said method describing: (a) receiving an item that is presented to the device (reference provided to determine cache hit/miss (Jouppi, page 43, section 8)); and (b) verifying whether said received item is already present in said device (Detecting cache hit/miss (Jouppi, page 43, section 8)); if said verification is negative, memorizing said received item in the device (Detecting cache hit/miss (Jouppi, page 43, section 8)). Jouppi does not specifically describe that the first memory stores the M items that were last presented to said device, that an oldest

of said M items in said first memory being moved to said second memory if said first memory already contains M items when a first item is presented for memorization, that the first item becomes a newest of said M items in said first memory or that if verification is positive that the received item is designated as an item last memorized in said device.

Bryant describes that one replacement algorithm is LRU (least recently used), whereby the block in the buffer which was referenced least recently (i.e. longest not used) is assumed to be the least important, and therefore can be written over, i.e. replaced with minimum system performance impact (column 1, lines 13 – 18). It is further known that in an LRU replacement scheme that an item that has just been referenced becomes the most recently used. Items removed from would be the oldest items that have been least recently used.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a LRU replacement algorithm as described by Bryant with the first memory of Jouppi because LRU provides performance benefits by replacing items which have been deemed to be least important because they have been least recently used (column 1, lines 13 – 18).

Regarding claim 7, Jouppi in view of Byrant describe the method according to claim 6, further comprising if said verification in step (b) is negative: if said first memory does not already contain M items, memorizing said received item in said first memory (Jouppi, page 43, section 8); if said first memory already contains M items, transferring said oldest of said M items to said second memory

(LRU of Bryant teaches that the oldest least recently used data should be removed since it is least important (column 1, lines 13 – 18)) (first-level victim of Jouppi, page 43, section 8); and if said second memory already contains N-M items, randomly selecting one of said second items in said second memory for removal from said second memory, removing said randomly selected item, and memorizing said oldest of said M items in said second memory (pseudo random replacement of Jouppi, page 35, section 2.5).

Regarding claim 8, Jouppi in view of Bryant describe the device according to claim 2 (see above), wherein if said first item is already present in said device, said oldest item in said first memory is moved to said second memory and said first item is moved from said second memory to said first memory as said newest of said M items in said first memory (When a reference misses in the first level and hits in the second the contents of the first-level cache line are transferred to the second-level cache and the second-level cache is used to refill the first-level cache (Jouppi, page 43, section 8). LRU of Bryant would teach that the least recently used data would be removed from the first level and the new data coming from the second level would be the newest (most recently used)).

4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi in view of Bryant as applied to claim 1 above, further in view of Vishlitzky et al. US Patent No. 5513336 (herein after referred to as Vishlitzky).

Regarding claims 4 and 5, Jouppi in view of Bryant describe the device according to claim 1 (see above). They do not specifically describe said device

being adapted to memorize the number of times that said first item has been presented to said device or that said device being adapted to supply information indicating whether said first item has already been presented to said device for a number of times that exceeds a predetermined number.

Vishlitzky describes the use of an access counter which is examined to determine how many times the data element has been accessed (column 16, lines 14 – 26). Examination of the access counter can determine if a data element has been accessed more than some number of times.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the access counter as described by Vishlitzky with the invention of Jouppi in view of Bryant because an access counter can determine the most or least recently used data in order to determine data that should be replaced upon a cache miss.

***Response to Arguments***

Applicant argues that there is no proper motivation or suggestion to combine Jouppi with Bryant as done by the Examiner. Examiner submits that LRU replacement algorithm is a well known replacement algorithm and the motivation for to use an LRU replacement scheme has actually appeared in the Bryant reference (column 1, lines 13 – 18).

Applicant argues that one skilled in the art would not have been motivated to use a different replacement algorithm with each memory. Examiner submits that one of ordinary skill in the art would have been aware of the benefits of both

replacement algorithms and would be motivated to use a combination of the two in order to gain benefits from both such as the very good cache performance of LRU replacement and the simplicity of Random replacement.

Applicant argues that Jouppi does not describe how the item in the first cache is chosen for removal nor does it describe what happens if the second cache does not have sufficient capacity to receive the item from the first cache. Examiner has used Bryant to describe that the removal from a first memory could be based on a least recently used replacement algorithm and therefor the oldest least recently used entry would be chosen for removal. Furthermore the Examiner submits that Jouppi teaches that pseudo-random replacement is used with the second-level cache and therefore when the second-level is full and therefore needs to choose a candidate for replacement it is randomly chosen and replaced (page 35, section 2.5).

Applicant argues that Bryant does not describe removing the oldest item from the first memory and moving it to a second memory. Examiner submits that a LRU scheme teaches that the oldest least recently used entry is chosen for replacement or removal. As newer entries are referenced a first referenced entry becomes the oldest and least recently used.

Applicant argues that dependent claims are allowable for the reasons argued above. Examiner refers to the above responses to said arguments as to why these reasons do not make the claims allowable.

***Conclusion***

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ralph A. Verderamo III whose telephone number is (571) 270-1174. The examiner can normally be reached on M-Th 7:30 - 5, every other Friday 7:30-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ralph A. Verderamo III
Examiner
Art Unit 2186

rv
January 15, 2008

sjt 1/17/08

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